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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/259,179 | 02/26/1999 | STANLEY A. SCHNEIDER | REALP001 | 4970 |

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| EXAMINER | |
|---|---|
| INGBERG, TODD D | |
| ART UNIT | PAPER NUMBER |
| 2124 | 18 |

DATE MAILED: 08/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/259,179 | SCHNEIDER ET AL. | |
| | Examiner | Art Unit | |
| | Todd Ingberg | 2124 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *51-73* is/are pending in the application.

4a) Of the above claim(s) *1-50* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *51-73* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

Claims 1 - 50 have been canceled.

Claims 51 - 73 have been added.

### *Request For Continued Examination*

1. The Request for a Continued Examination (RCE) has been entered.

### *Claim Rejections - 35 U.S.C. § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 51 - 73 are rejected under 35 U.S.C. 102(b) based upon a public use or sale of the invention. ControlShell 5.1 released June 1996.

ControlShell 5.1 with it's object oriented implementation ( Chapter 1 - Introduction) anticipates the hierarchial structure and multi hierarchy with a set of components. Naming components (page 5-8) and defining modes as in the finite state machine engine (chapters 8 and the editor of chapter 9) and code generation from the FSM editor (page 9-43). Running of the executable FSM where the model is one mode is not able to access features of another mode is inherent in programming control systems.

*Claim Rejections - 35 U.S.C. § 102*

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 51 - 73 are rejected under 35 U.S.C. 102(b) as anticipated by VOOP or, in the alternative, under 35 U.S.C. 103(a) as obvious over Visual Object-Oriented Programming Concepts and Environments by M. M. Burnett et al. (called **VOOP**) in view of Visual Basic 6.0 as documented in the September 1998 Manual "Visual Basic 6 Unleashed" (called **VB**).

**Claim 51**

**VOOP** teaches a method of defining modes of operation for, and mapping said modes through, a hierarchical system, wherein said hierarchical system comprises a multi-level hierarchy, with a set of components at each level, said method comprising defining one or more modes at each level by

a. identifying an intuitive name for a mode; and

b. choosing a subset of said set of components in said level; and

c. choosing a sub-mode for each chosen component, so that said mode is deed by the sub-modes of the chosen components, where in the simplest (end condition) case, said sub-mode indicates if the component is active or not, whereby when said level is executing in said mode,

d. Repeating steps a-c until modes defined at any level in the hierarchy are mapped to sub-modes down the hierarchy, whereby when said hierarchy is executing, (**VOOP**, VIPR, pages 70 - 90 and page 159, Chapter 2 - real world systems, pages 216 - 225 and chapter 8 languages).

***** Grounds of 103 *****

**VOOP** does not explicitly teach that "only active components will execute throughout the hierarchy" and viewing the book the pages are static it is not easy to see the actual feel of the product. However, it is well known that in **VB** "only active components will execute" (**VB**, page 304 , an example of the use of greying out features not available in this state.). One of ordinary skill in the art of building development tools at the time of invention would have thought to combine the teachings of VOOP with VB. Given the teachings of VOOP on building object oriented control systems and the explicit teaching of VB where features in different states have different features available and the VB programming environment allows one to enforce these state mode rules it would have been obvious because making the model conform to the behavior of the real system is critical in program solutions.

***** Grounds for 102 *****

**VOOP** pages 166 - 167 teach the importance of sequencing and modification ("only active components will execute") and also further support the motivation provided for the 103 rejection above.

**Claim 52**

A method as recited in claim 51 wherein said hierarchical system is a control system (**VOOP**, page 221 figure 10.8).

**Claim 53**

A method as recited in claim 51 wherein said hierarchical system is a real-time control system.(**VOOP**, page 221 figure 10.8 and object oriented by definition).

**Claim 54**

A method as recited in claim 51 wherein said components are represented in a graphical user interface and said choosing said subset of components includes selecting said sub-modes using said graphical user interface (**VOOP**, page 221 figure 10.8).

**Claim 55**

A method as recited in claim 51 wherein said components are represented in a graphical user interface and said choosing said submodes includes selecting said subset of components using said graphical user interface, whereby said subset of components are visually distinguished from components not in said subset.(**VOOP**, page 221 figure 10.8 - Categories).

**Claim 56**

A method as recited in claim 51 wherein said hierarchical system is a control system, and said components are executing said control system on a computer.(**VOOP**, page 221 figure 10.8).

**Claim 57**

A method as recited in claim 56 further comprising: switching from said mode to a different mode while said control system is executing; deactivating those components that correspond to

said mode; and activating those components that correspond to said different mode. As per independent claim 51 above.

**Claim 58**

A method of mapping a thread of a processor to components within a control system, wherein said control system comprises a plurality of components in a multi-level hierarchy (**VOOP**, Object oriented by definition) , said method comprising:

a. defining one or more logical rates of execution at each level in said multi-level hierarchy;

b. for each component in a level of said multi-level hierarchy, assigning said component to one or more of said logical rates (**VOOP**, page 28 figure 2.3 shows Delays which control rates - bit rates); and

c. mapping said thread of said processor to one or more of said logical rates, thus mapping said thread through said multi-level hierarchy, resulting in a system of components, executing at the actual execution rate of said thread. (**VOOP**, page 28 figure 2.3 - executable objects map to threads).

*** basis for 103 ***

The basis of the rejection is the functionality of the grounds of rejection as taught in claim 1 in view of the explicit teaching of threads in VB chapter 9. Threads are inherent in program

executables. The motive to combine the inherent need to have threads for a control system of VOOP with the built in thread control features of VB is inherent and can not be separated.

*** basis for 102 ***

(**VOOP**, page 28 figure 2.3 - executable objects map to threads).

**Claim 59**

A method as recited in claim 58 wherein said control system is a real-time control system. (**VOOP**, page 28, control for a telemetry system being modeled).

**Claim 60**

A method as recited in claim 58 wherein said components are represented in a graphical user interface and said process of assigning includes selecting components at each level using said graphical user interface, arid defining said logical rates of execution using said graphical user interface. (**VOOP**, page 28, modeling on a GUI).

**Claim 61**

A method as recited in claim 58 wherein said components are executing on a real-time computer.(**VOOP**, page 28, control for a telemetry system being modeled).

**Claim 62**

A method as recited in claim 58 wherein multiple threads are mapped to multiple components, wherein each component may be assigned one or multiple logical rates and each said logical rate

mapped to a thread. (**VOOP**, page 28, control for a telemetry system being modeled - both delays and bit rates ).

**Claim 63**

A method of defining an executable image for a control system comprising a plurality of components, said method comprising

a. choosing a subset of said components to correspond to said executable image;

b. identifying a name for said executable image ( The object name is the name of the executable in most systems the object name followed by a number giving it a unique ID is the image ID) and its corresponding subset of said components; and

c. for each chosen component in said subset, indicating that said component is part of said executable image for said control system, whereby when said executable image is produced for said control system, only said subset of said components that correspond to said executable image will be included. As per claim 58 above

**Claim 64**

A method as recited ire claim 63 wherein said control system is an electromechanical control system( **VOOP**, pages 28 - 30, Galileo Telemetry system).

**Claim 65**

A method as recited in claim 63 wherein said control system is a real-time control system. ( **VOOP**, pages 28 -Telemetry system).

**Claim 66**

A method as recited in claim 63 wherein said received components are represented in a graphical user interface and said element of choosing includes selecting said subset of components using said graphical user interface, whereby said subset of components are visually distinguished from components not in said executable image. As per claim 51.

**Claim 67**

A method as recited in claim 63 further comprising:

a. loading components corresponding to said executable image into a real-time computer; and

b . executing said executable image on said real-time computer. As per claim 58.

**Claim 68**

A method as recited in claim 63 whereby multiple executable images are generated, each destined for a different particular computer.

**Interpretation** - given the broadest reasonable interpretation the ability to generate a solution for a telemetry system and then use the tool for a another solution is not excluded from the interpretation of the reference. On page 74 of VOOP the C++ language is mentioned. It is well known to be able to run an executable on different computers. The limitation "particular" is not distinguishing the invention.

**Claim 69**

A method of defining an executable image for a control system, wherein said control system comprises a multi-level hierarchy, said method further comprising:

a. defining at least one logical executable name or designator at each level;

b. choosing a subset of components at each level to correspond to each said logical executable name;

c. for each chosen component in each subset, indicating that said component is part of said logical executable name;

d. continuing this process throughout the hierarchy, thus assigning components to logical executable names at each level; and

e. mapping said executable image to said logical executable names throughout said multi-level hierarchy such that only the subset of said components assigned to the mapped said logical executable names will be included in the executable image. As per claim 63.

**Claim 70**

A method as recited in claim 69 wherein said control system is a real-time control system. As per claim 65.

**Claim 71**

A method as recited in claim 69 wherein said components are represented in a graphical user interface and said element of choosing includes selecting said subset of components using

said graphical user interface, whereby said subset of components are visually distinguished from components not in said executable image. As per claim 66.

**Claim 72**

A method as recited in claim 69 further comprising: a. loading components corresponding to said executable image into a real-time computer; and b. executing said executable image on said real-time computer. As per claim 63.

**Claim 73**

A method as recited in claim 69 whereby multiple executable images are generated, each destined for a different particular computer. As per claim 68.

***Allowable Subject Matter***

5. It was the Examiner's understanding from the Interview that the feature involving the parameters to the COG were novel to the inventors product (version 6.0) and would be in the claimed invention. The Examiner believes the feature to be part of the Intelligent Control Interface. This is not seen in the claims.

***Conclusion***

6. What the Examiner sees in the claims is the functionality of being able to control feature availability based on the state of the model. In programming languages such as Visual Basic™ and C++ the ability to grey out features such as a cascade menu based on the state of the model is old and well known. In a practical example of state and available feature a word processor such as Microsoft Word in the edit menu shows the feature paste greyed out if the state of the paste buffer is empty. If a copy or cut operation is performed the state of the paste buffer is changed and the feature paste is no longer greyed out. Although, the example is simple it is the basic concept implemented in state transition sequencing and feature availability. The Gomaa reference the Examiner made of record with the Interview summary teaches the relationship between state transition and the available modes. Many of the examples of Gomaa are also scenarios in the Assignee's documentation. It appears the claim language is so broad it reads in version 5.1 of Assignee's product.

## *Correspondence Information*

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Todd Ingberg** whose telephone number is **(703) 305-9775.** The Examiner is working a Maxi-Flex schedule and can be reached Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the **Examiner's Supervisor, Kakali Chaki** be reached at **(703)305-9662.** Any response to this office action should be mailed to: **Director of Patents and Trademarks Washington, D.C. 20231**, or **Hand-delivered** responses should be brought to **Crystal Park II, 2121 Crystal Drive Arlington, Virginia, (Receptionist located on the fourth floor),** or **faxed.** The following **fax numbers** apply:

| | |
|---|---|
| **Official** | **(703) 746 - 7239** |
| **Non Official/ Draft** | **(703) 746 -7240** |
| **After Final** | **(703) 746 - 7238** |

**Todd Ingberg**
Primary Examiner
Art Unit 2124
August 10, 2003